FIG. 1

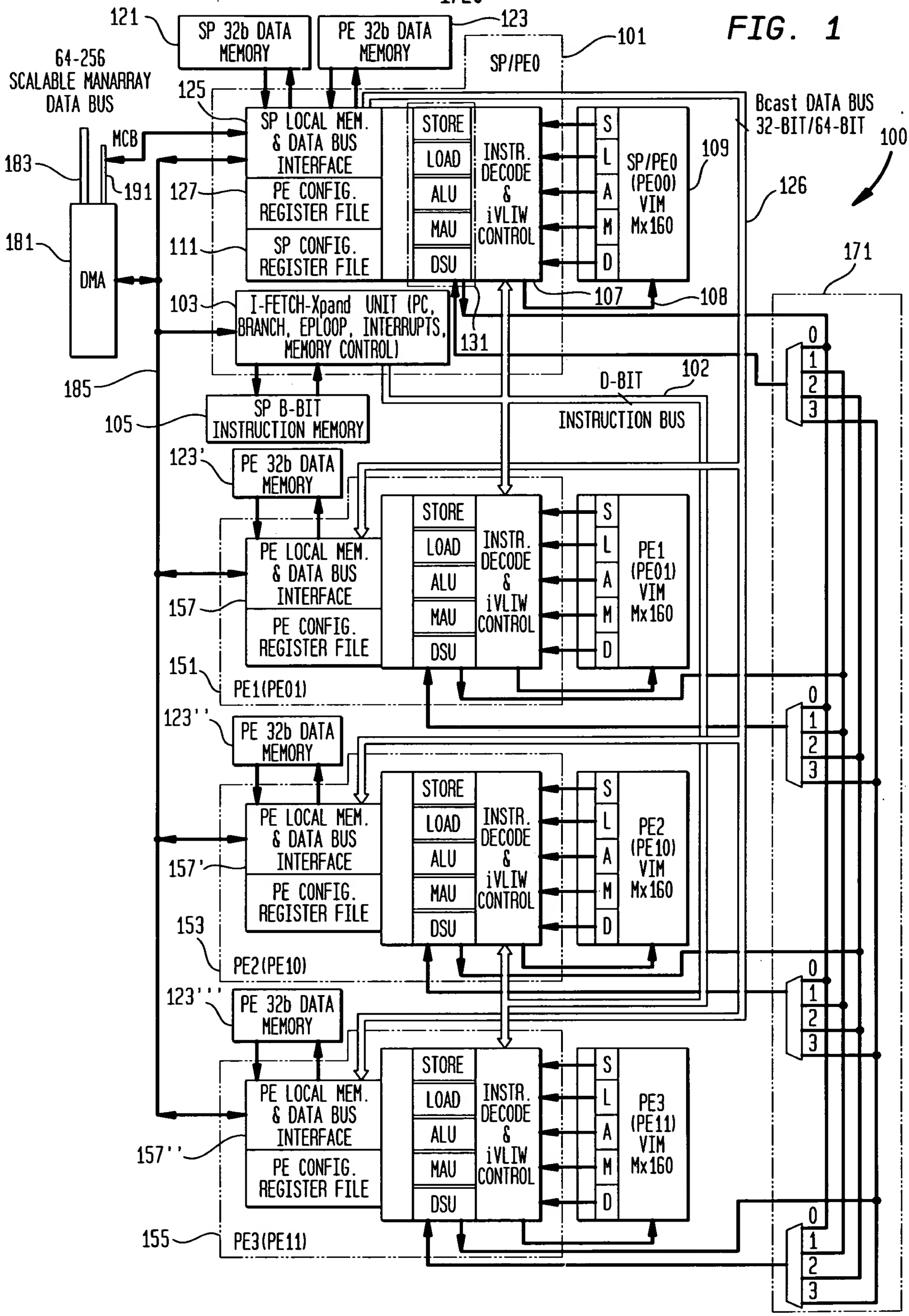

121
SP 32b DATA MEMORY
123
PE 32b DATA MEMORY
101
SP/PE0
64-256 SCALABLE MANARRAY DATA BUS
125
SP LOCAL MEM. & DATA BUS INTERFACE
STORE
LOAD
ALU
MAU
DSU
INSTR. DECODE & iVLIW CONTROL
S
L
A
M
D
SP/PE0 (PE00) VIM Mx160
109
Bcast DATA BUS 32-BIT/64-BIT
100
126
MCB
183
191
127
PE CONFIG. REGISTER FILE
181
DMA
111
SP CONFIG. REGISTER FILE
171
103
I-FETCH-Xpand UNIT (PC, BRANCH, EPLOOP, INTERRUPTS, MEMORY CONTROL)
107
108
131
0
1
2
3
185
102
D-BIT
INSTRUCTION BUS
105
SP B-BIT INSTRUCTION MEMORY
123'
PE 32b DATA MEMORY
PE LOCAL MEM. & DATA BUS INTERFACE
157
PE CONFIG. REGISTER FILE
PE1 (PE01) VIM Mx160
151
PE1(PE01)
123''
PE 32b DATA MEMORY
157'
PE2 (PE10) VIM Mx160
153
PE2(PE10)
123'''
PE 32b DATA MEMORY
157''
PE3 (PE11) VIM Mx160
155
PE3(PE11)

FIG. 1B

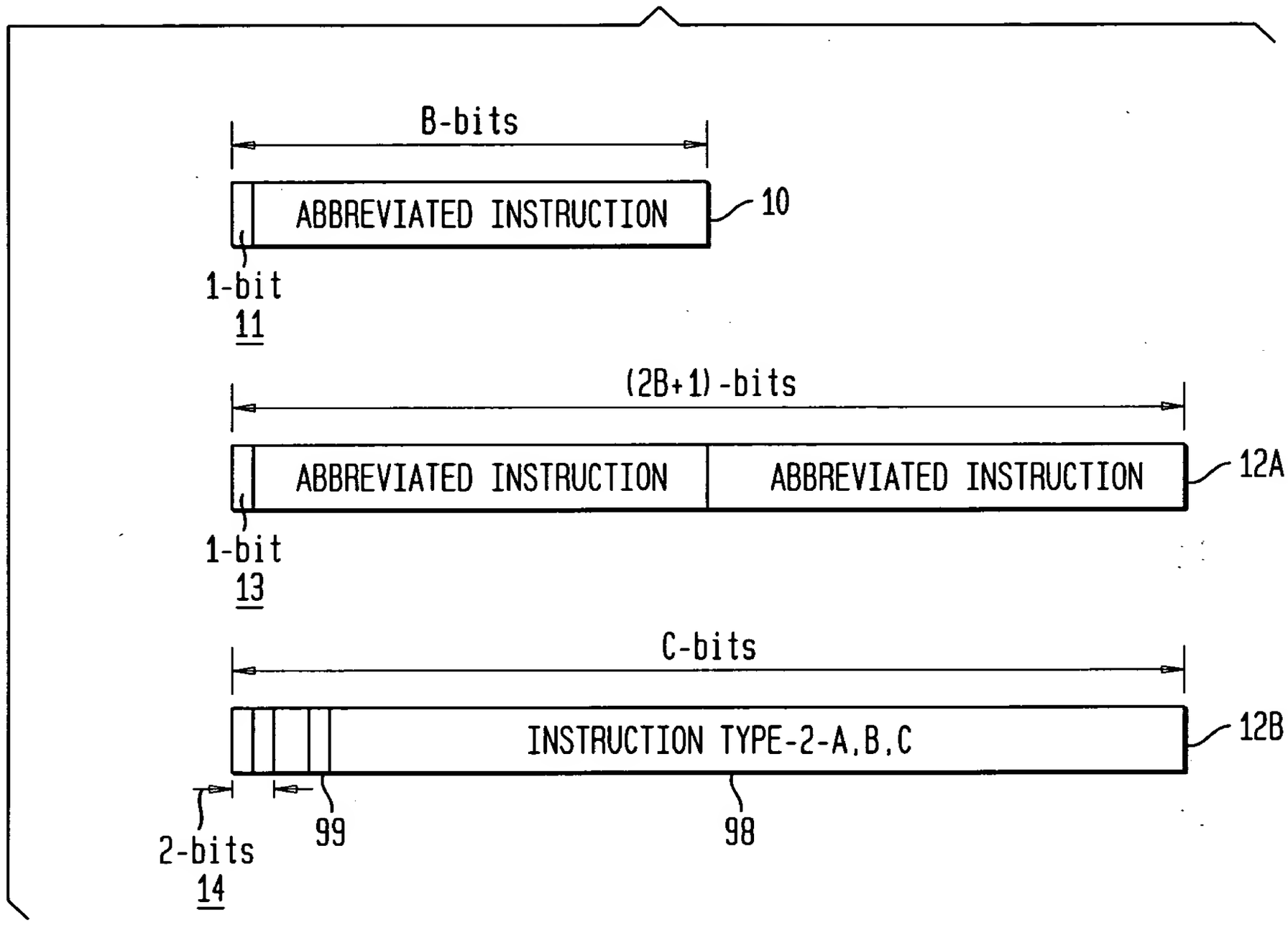

B-bits
ABBREVIATED INSTRUCTION
10
1-bit
11
(2B+1)-bits
ABBREVIATED INSTRUCTION
ABBREVIATED INSTRUCTION
12A
1-bit
13
C-bits
INSTRUCTION TYPE-2-A,B,C
12B
2-bits
14
99
98

FIG. 2

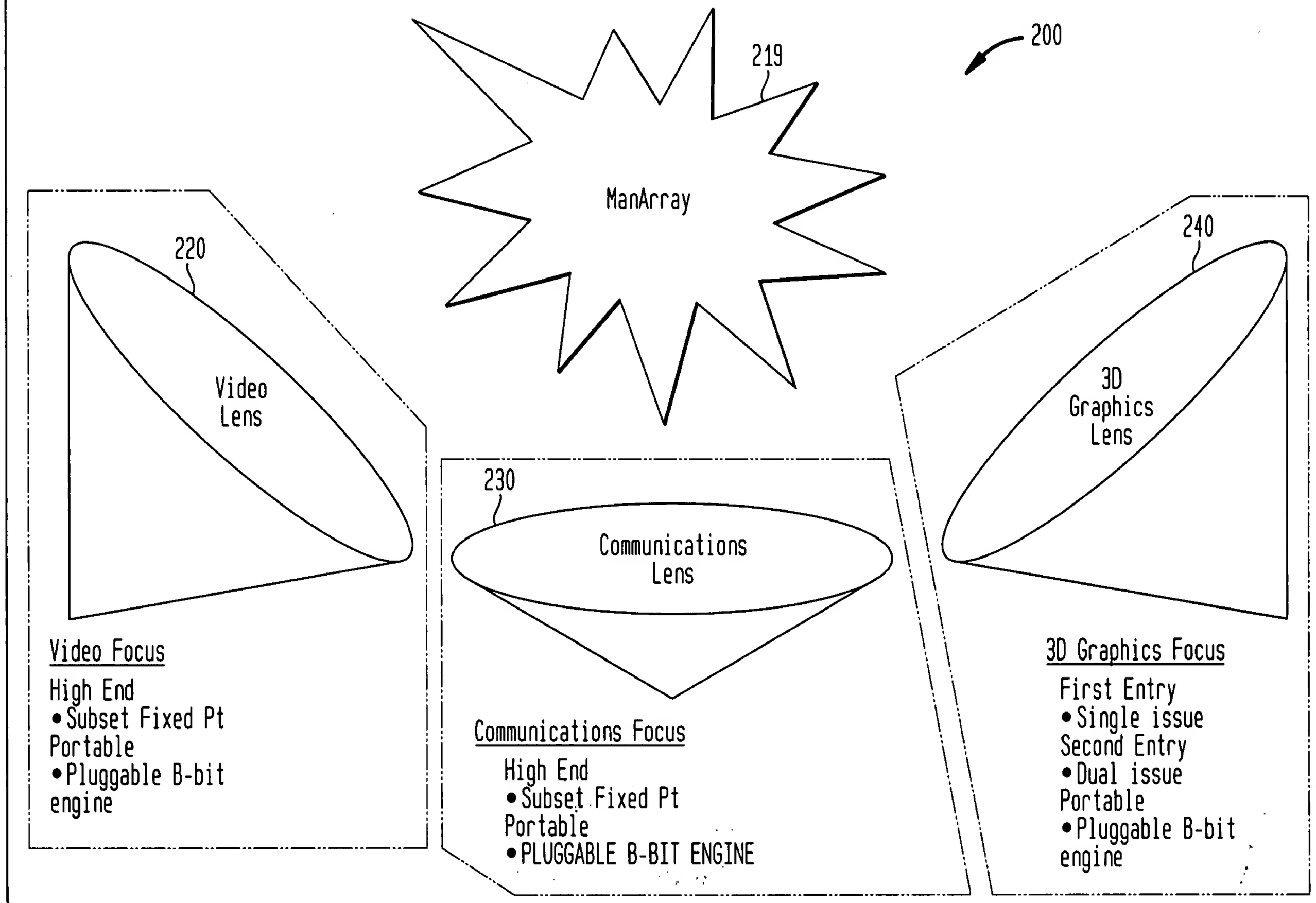

200
219
ManArray
220
Video
Lens
240
3D
Graphics
Lens
230
Communications
Lens
Video Focus
High End
• Subset Fixed Pt
Portable
• Pluggable B-bit
engine
Communications Focus
High End
• Subset Fixed Pt
Portable
• PLUGGABLE B-BIT ENGINE
3D Graphics Focus
First Entry
• Single issue
Second Entry
• Dual issue
Portable
• Pluggable B-bit
engine

FIG. 3A

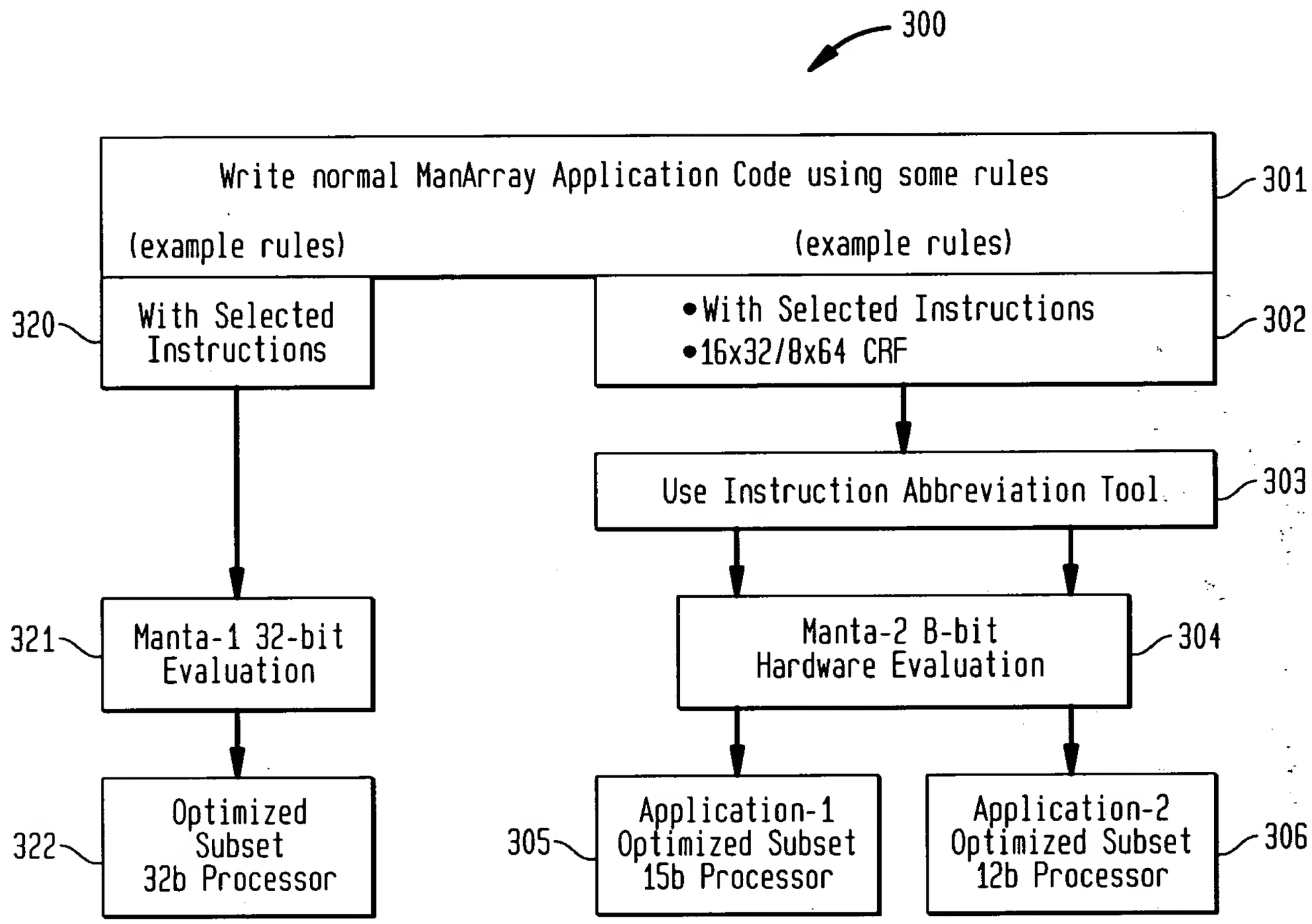

300
Write normal ManArray Application Code using some rules
301
(example rules)
(example rules)
320
With Selected Instructions
•With Selected Instructions
•16x32/8x64 CRF
302
Use Instruction Abbreviation Tool
303
321
Manta-1 32-bit Evaluation
Manta-2 B-bit Hardware Evaluation
304
322
Optimized Subset 32b Processor
305
Application-1 Optimized Subset 15b Processor
Application-2 Optimized Subset 12b Processor
306

FIG. 3B

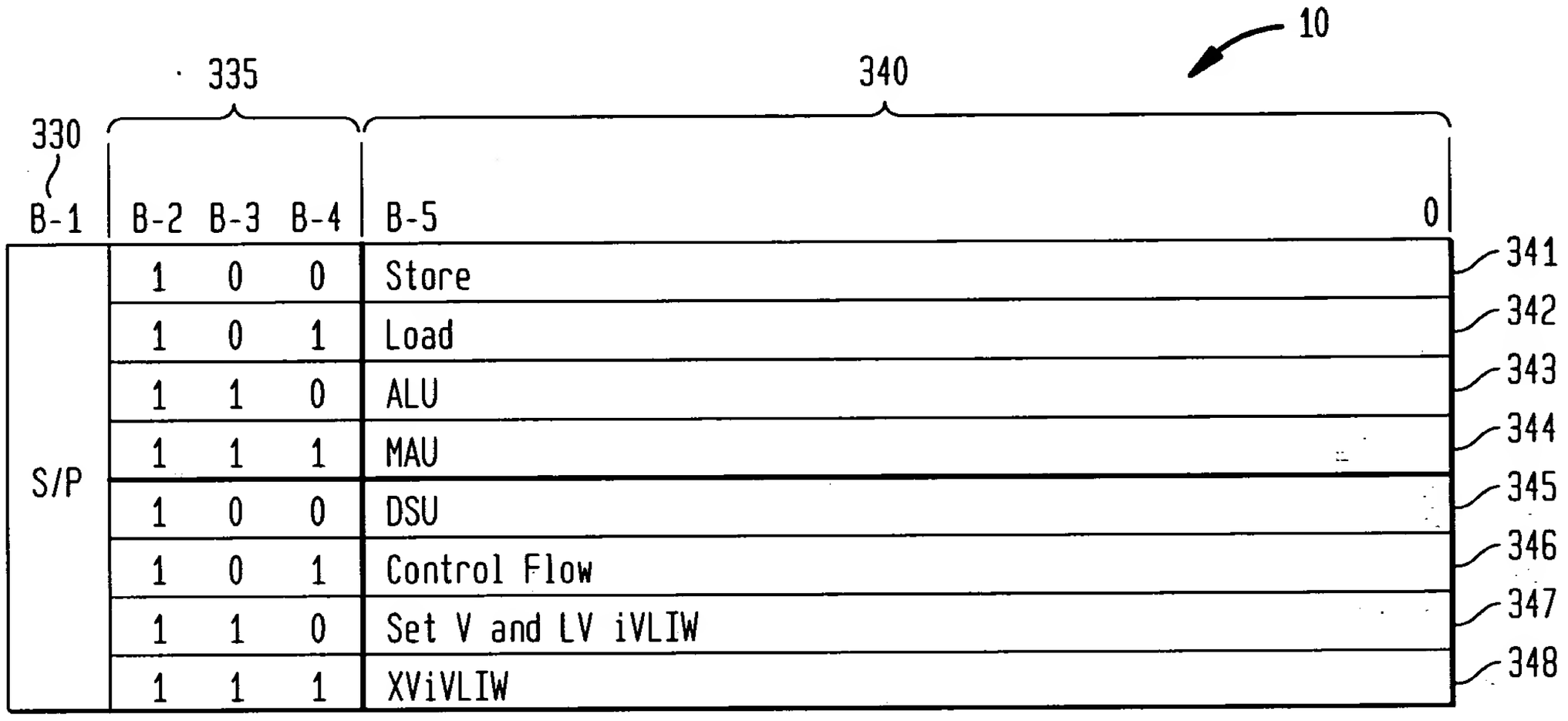

10
335
340
330
B-1
B-2 B-3 B-4
B-5
0
S/P
1 0 0 Store
1 0 1 Load
1 1 0 ALU
1 1 1 MAU
1 0 0 DSU
1 0 1 Control Flow
1 1 0 Set V and LV iVLIW
1 1 1 XViVLIW
341
342
343
344
345
346
347
348

FIG. 3C

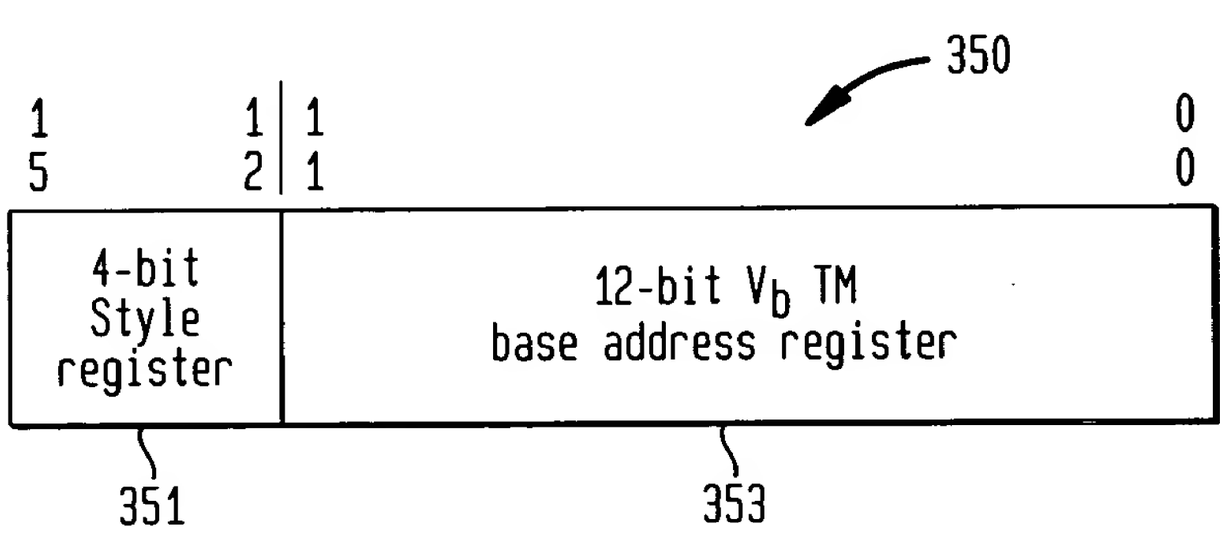

350
15
12
11
0
0
4-bit
Style
register
12-bit V_b TM
base address register
351
353

FIG. 3D

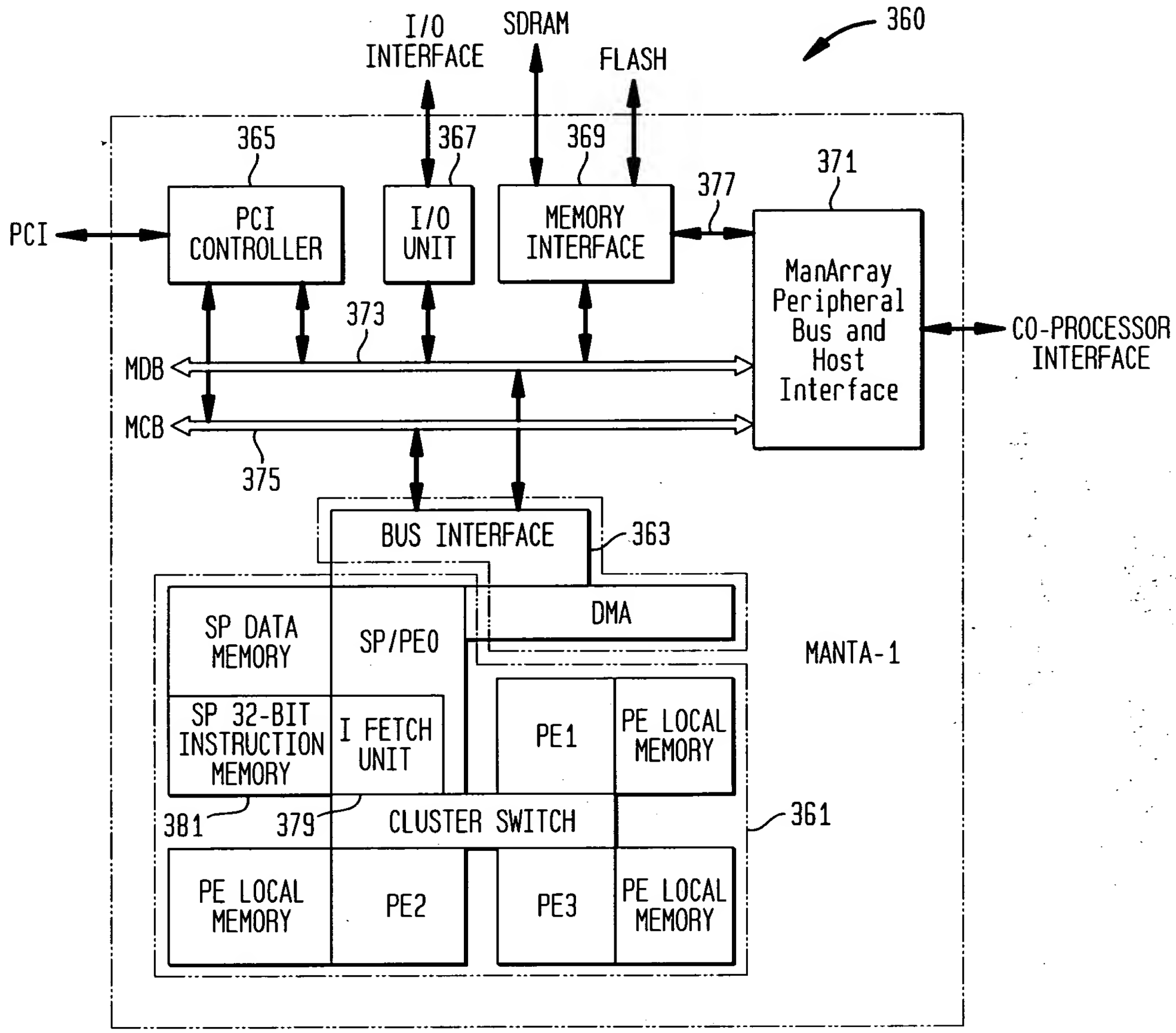
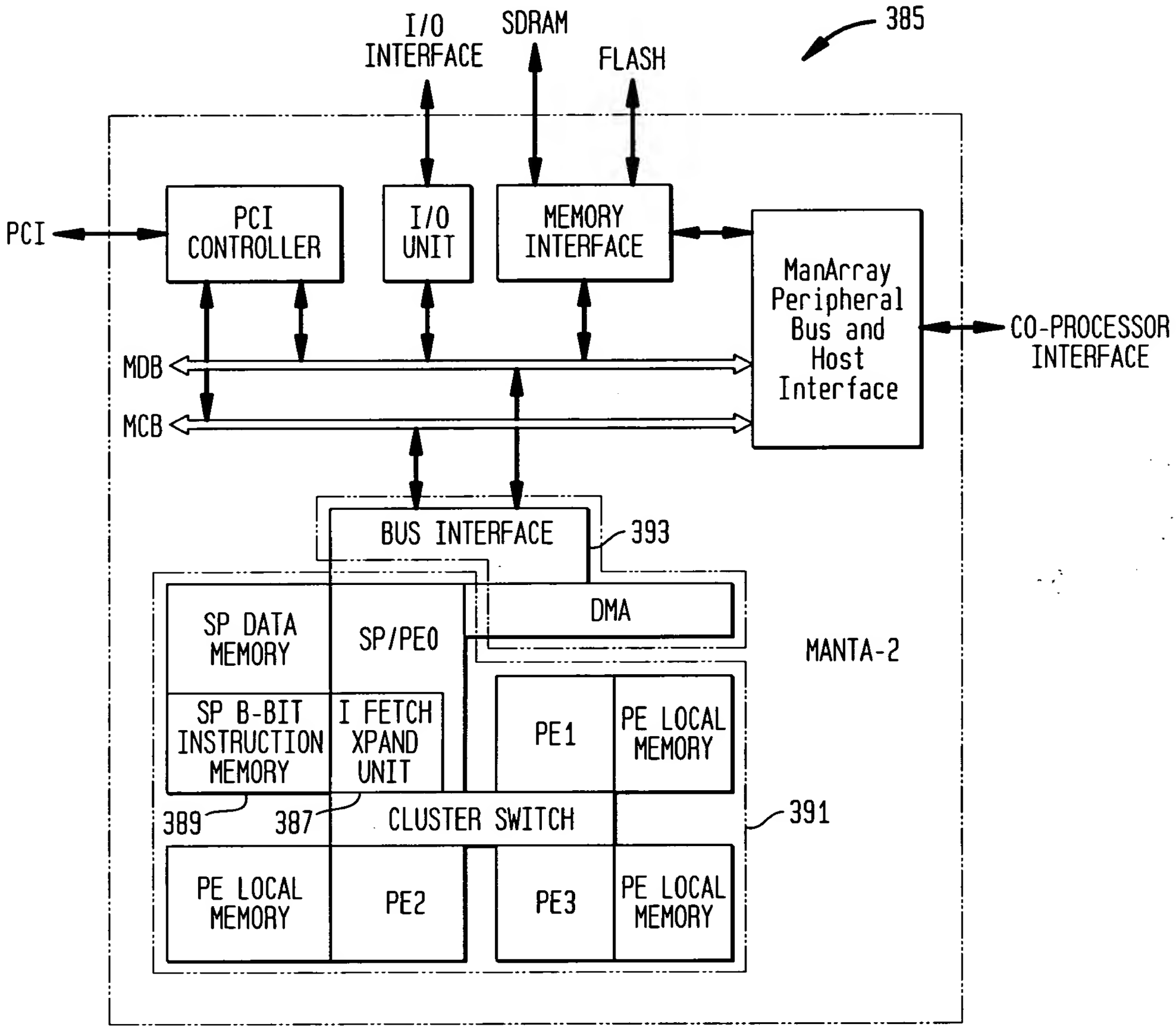

360
I/O INTERFACE
SDRAM
FLASH
365
367
369
371
377
PCI
PCI CONTROLLER
I/O UNIT
MEMORY INTERFACE
ManArray Peripheral Bus and Host Interface
CO-PROCESSOR INTERFACE
373
MDB
MCB
375
BUS INTERFACE
363
SP DATA MEMORY
SP/PE0
DMA
MANTA-1
SP 32-BIT INSTRUCTION MEMORY
I FETCH UNIT
PE1
PE LOCAL MEMORY
381
379
CLUSTER SWITCH
361
PE LOCAL MEMORY
PE2
PE3
PE LOCAL MEMORY

FIG. 3E


385
I/O INTERFACE
SDRAM
FLASH
PCI
PCI CONTROLLER
I/O UNIT
MEMORY INTERFACE
ManArray Peripheral Bus and Host Interface
CO-PROCESSOR INTERFACE
MDB
MCB
BUS INTERFACE
393
DMA
SP DATA MEMORY
SP/PE0
MANTA-2
SP B-BIT INSTRUCTION MEMORY
I FETCH XPAND UNIT
PE1
PE LOCAL MEMORY
389
387
CLUSTER SWITCH
391
PE LOCAL MEMORY
PE2
PE3
PE LOCAL MEMORY

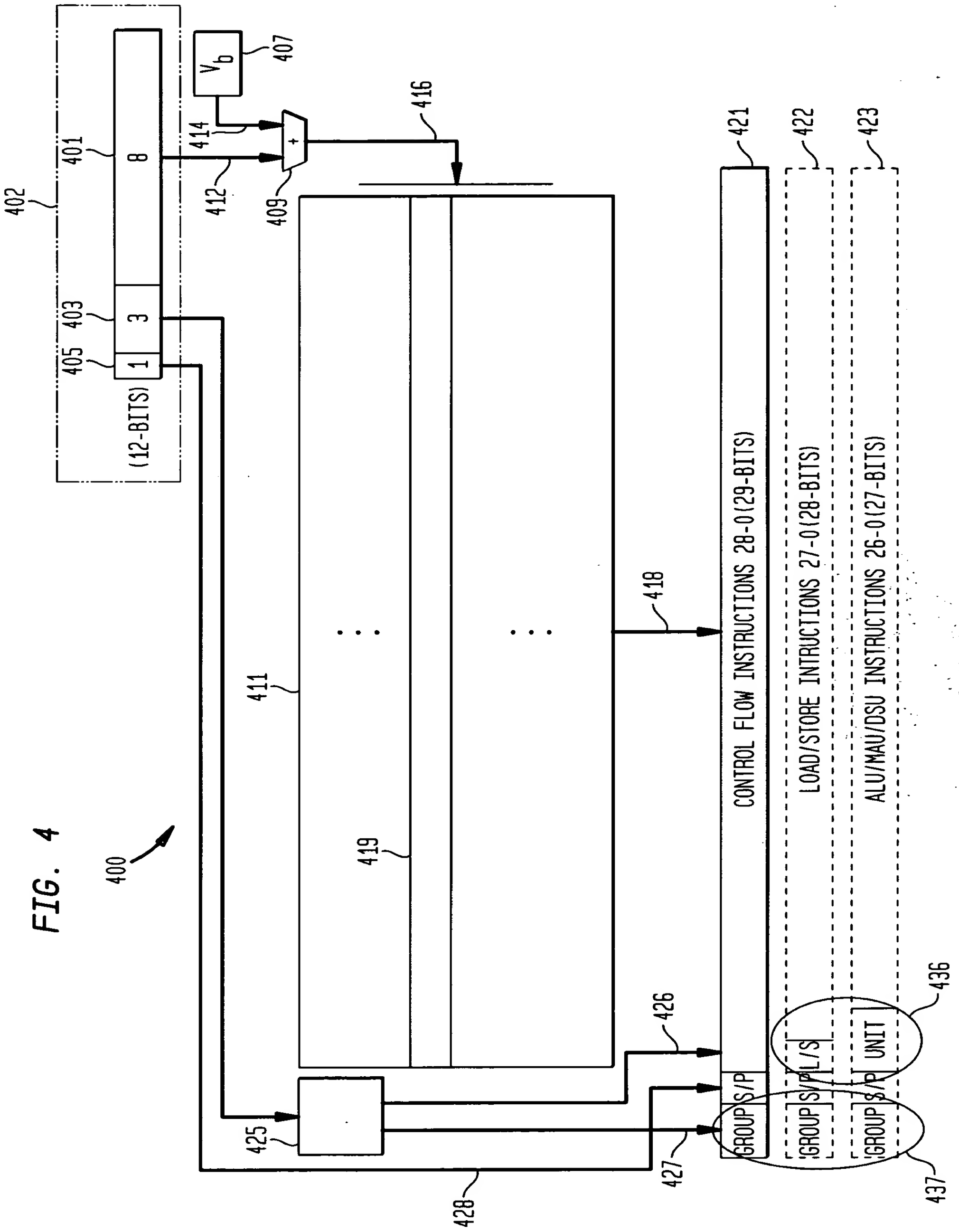

400
402
401
8
403
3
405
1
(12-BITS)
407
V_b
414
412
409
416
411
419
418
421
422
423
425
426
427
428
436
437
CONTROL FLOW INSTRUCTIONS 28-0(29-BITS)
LOAD/STORE INTRUCTIONS 27-0(28-BITS)
ALU/MAU/DSU INSTRUCTIONS 26-0(27-BITS)
GROUP
S/P
UNIT

FIG. 4

FIG. 5A

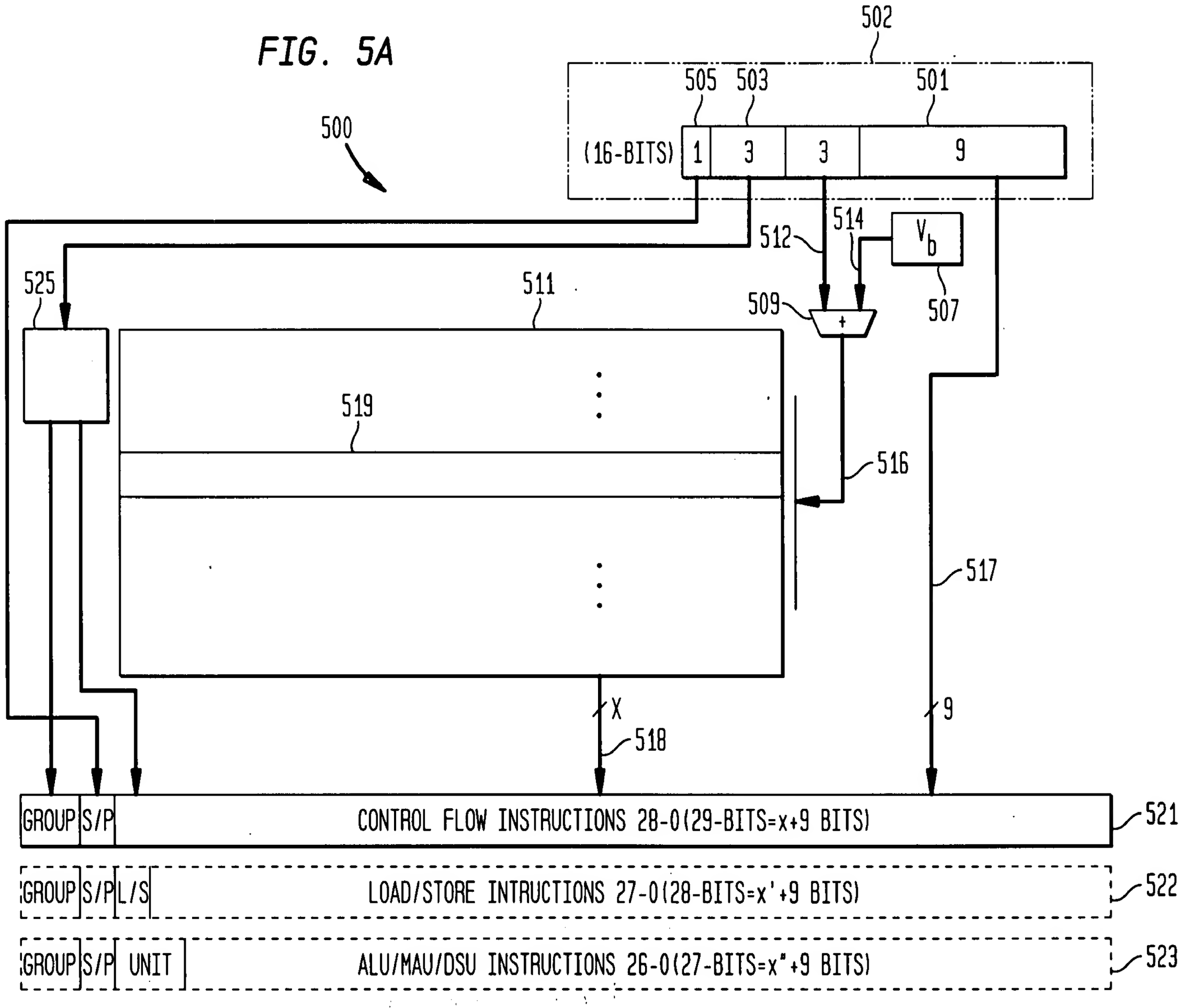

502
505
503
501
500
(16-BITS)
1
3
3
9
514
512
V_b
525
511
509
+
507
519
516
517
X
9
518
GROUP
S/P
CONTROL FLOW INSTRUCTIONS 28-0(29-BITS=x+9 BITS)
521
GROUP
S/P
L/S
LOAD/STORE INTRUCTIONS 27-0(28-BITS=x'+9 BITS)
522
GROUP
S/P
UNIT
ALU/MAU/DSU INSTRUCTIONS 26-0(27-BITS=x"+9 BITS)
523

FIG. 5B

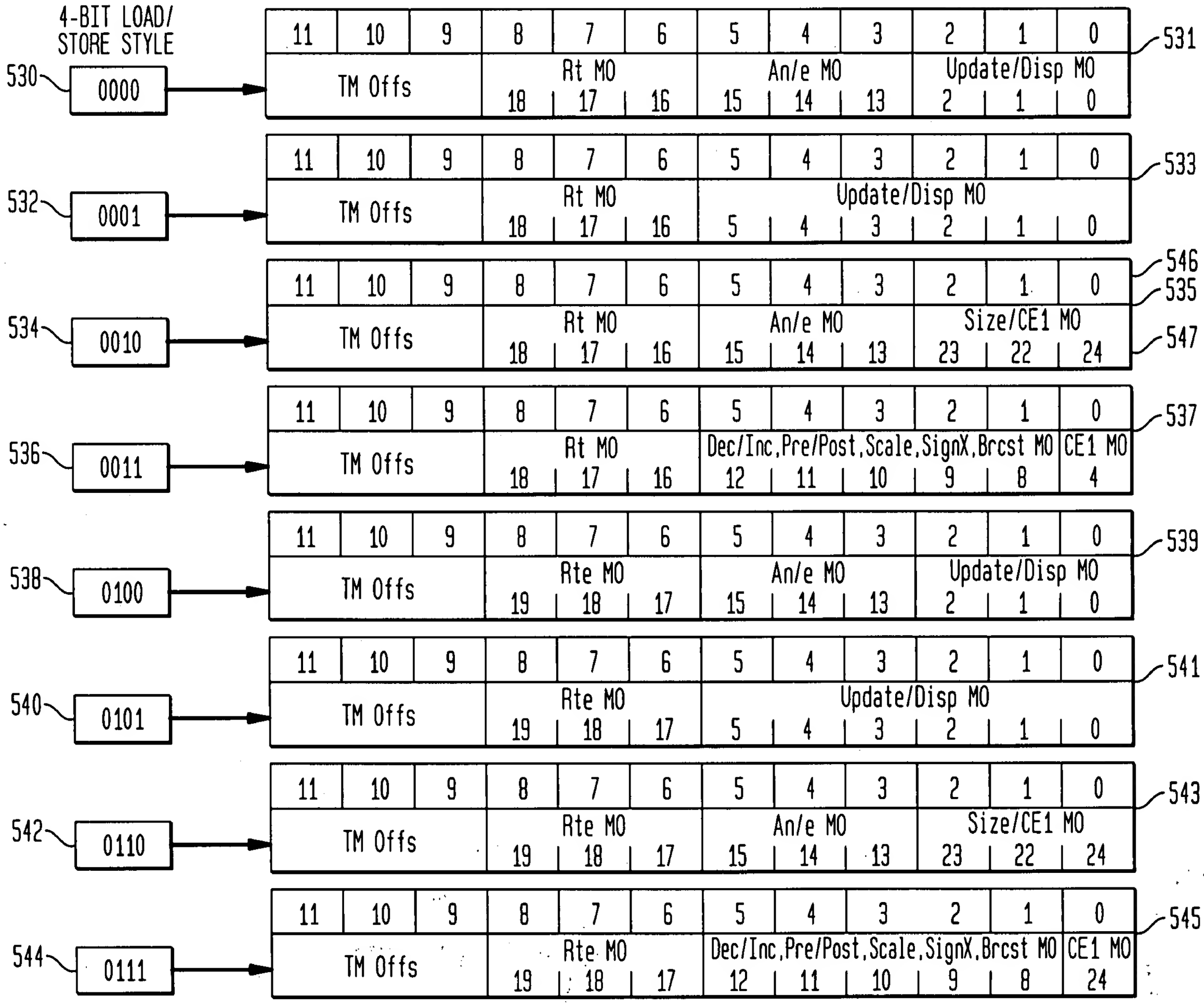

4-BIT LOAD/ STORE STYLE
530
0000
11 10 9 8 7 6 5 4 3 2 1 0
TM Offs
Rt M0 18 17 16
An/e M0 15 14 13
Update/Disp M0 2 1 0
531
532
0001
11 10 9 8 7 6 5 4 3 2 1 0
TM Offs
Rt M0 18 17 16
Update/Disp M0 5 4 3 2 1 0
533
534
0010
11 10 9 8 7 6 5 4 3 2 1 0
TM Offs
Rt M0 18 17 16
An/e M0 15 14 13
Size/CE1 M0 23 22 24
546
535
547
536
0011
11 10 9 8 7 6 5 4 3 2 1 0
TM Offs
Rt M0 18 17 16
Dec/Inc,Pre/Post,Scale,SignX,Brcst M0 12 11 10 9 8
CE1 M0 4
537
538
0100
11 10 9 8 7 6 5 4 3 2 1 0
TM Offs
Rte M0 19 18 17
An/e M0 15 14 13
Update/Disp M0 2 1 0
539
540
0101
11 10 9 8 7 6 5 4 3 2 1 0
TM Offs
Rte M0 19 18 17
Update/Disp M0 5 4 3 2 1 0
541
542
0110
11 10 9 8 7 6 5 4 3 2 1 0
TM Offs
Rte M0 19 18 17
An/e M0 15 14 13
Size/CE1 M0 23 22 24
543
544
0111
11 10 9 8 7 6 5 4 3 2 1 0
TM Offs
Rte M0 19 18 17
Dec/Inc,Pre/Post,Scale,SignX,Brcst M0 12 11 10 9 8
CE1 M0 24
545

FIG. 5C

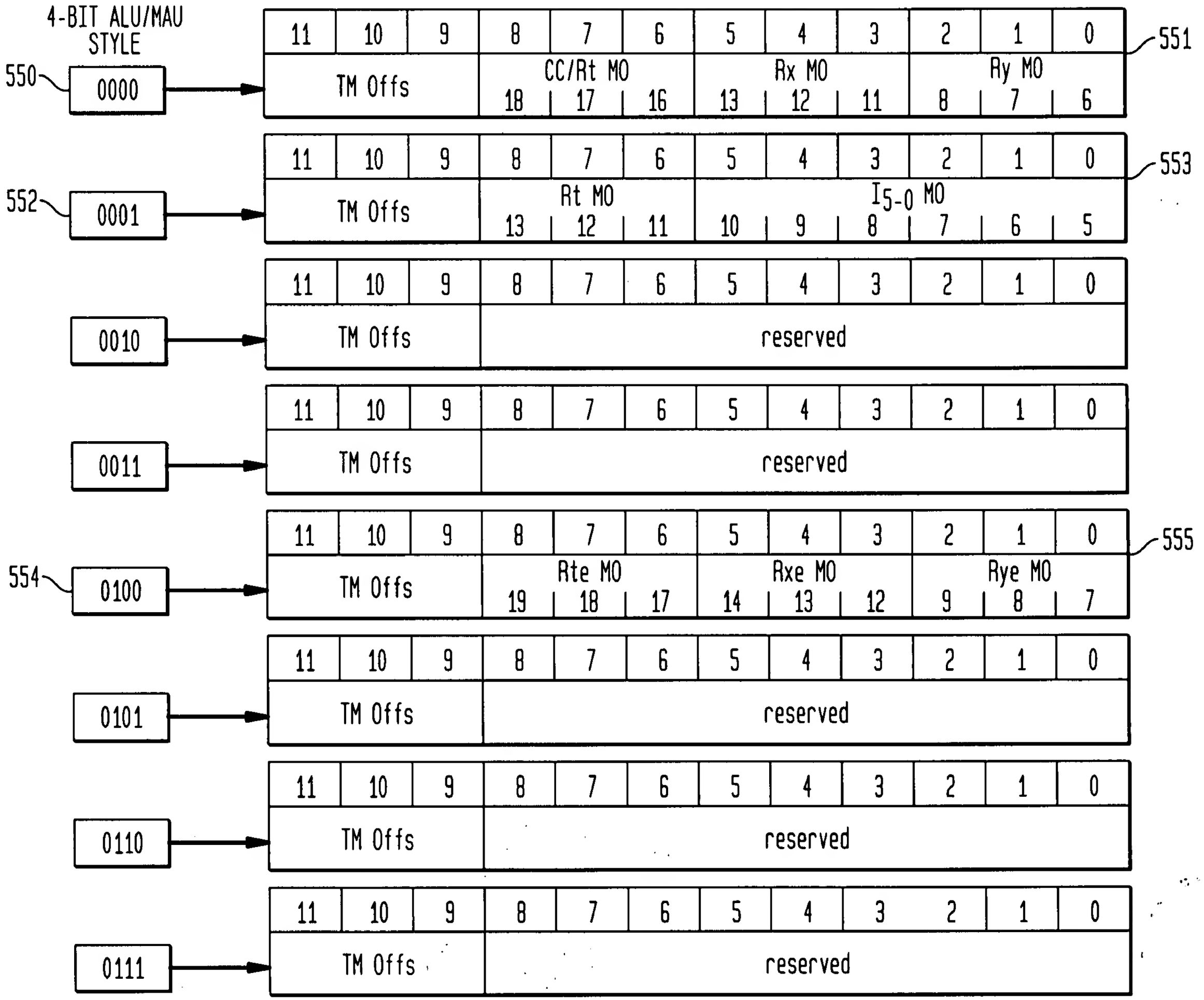

4-BIT ALU/MAU STYLE
550
0000
TM Offs
CC/Rt MO
18 17 16
Rx MO
13 12 11
Ry MO
8 7 6
551
552
0001
TM Offs
Rt MO
13 12 11
I5-0 MO
10 9 8 7 6 5
553
0010
TM Offs
reserved
0011
TM Offs
reserved
554
0100
TM Offs
Rte MO
19 18 17
Rxe MO
14 13 12
Rye MO
9 8 7
555
0101
TM Offs
reserved
0110
TM Offs
reserved
0111
TM Offs
reserved

FIG. 5D

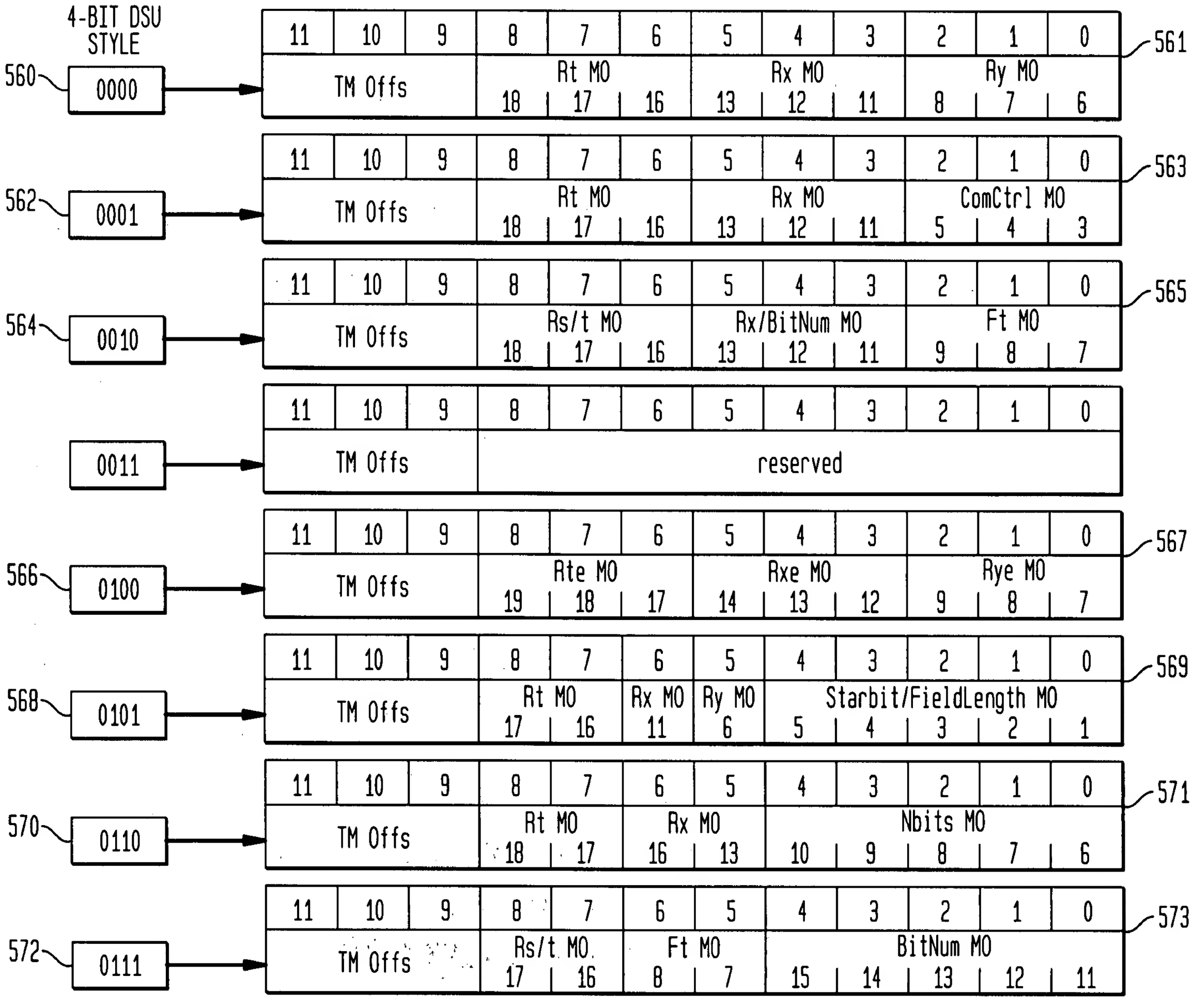
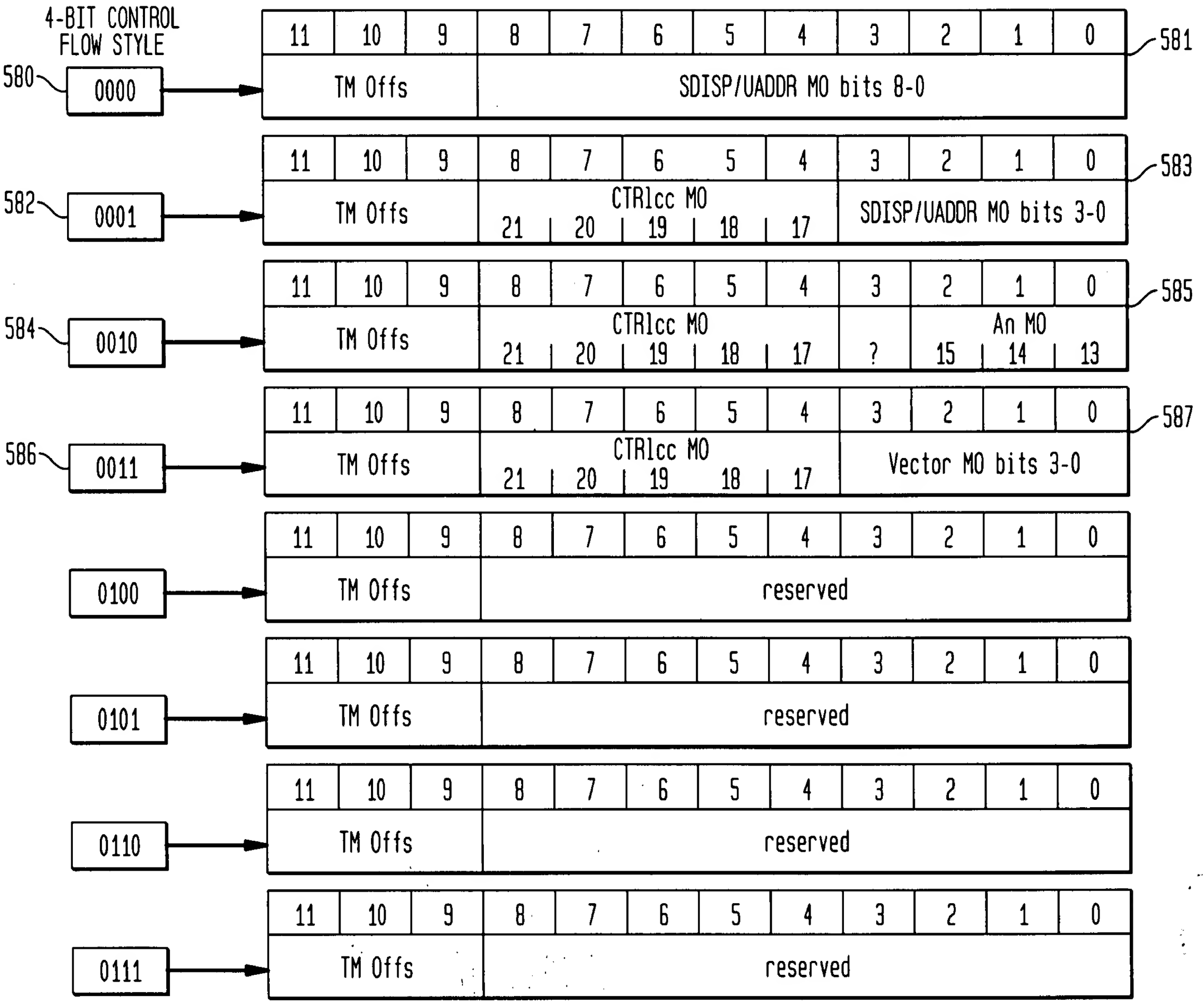

4-BIT DSU STYLE
560
0000
11 10 9 8 7 6 5 4 3 2 1 0
TM Offs
Rt MO 18 17 16
Rx MO 13 12 11
Ry MO 8 7 6
561
562
0001
11 10 9 8 7 6 5 4 3 2 1 0
TM Offs
Rt MO 18 17 16
Rx MO 13 12 11
ComCtrl MO 5 4 3
563
564
0010
11 10 9 8 7 6 5 4 3 2 1 0
TM Offs
Rs/t MO 18 17 16
Rx/BitNum MO 13 12 11
Ft MO 9 8 7
565
0011
11 10 9 8 7 6 5 4 3 2 1 0
TM Offs
reserved
566
0100
11 10 9 8 7 6 5 4 3 2 1 0
TM Offs
Rte MO 19 18 17
Rxe MO 14 13 12
Rye MO 9 8 7
567
568
0101
11 10 9 8 7 6 5 4 3 2 1 0
TM Offs
Rt MO 17 16
Rx MO 11
Ry MO 6
Starbit/FieldLength MO 5 4 3 2 1
569
570
0110
11 10 9 8 7 6 5 4 3 2 1 0
TM Offs
Rt MO 18 17
Rx MO 16 13
Nbits MO 10 9 8 7 6
571
572
0111
11 10 9 8 7 6 5 4 3 2 1 0
TM Offs
Rs/t MO 17 16
Ft MO 8 7
BitNum MO 15 14 13 12 11
573

FIG. 5E


4-BIT CONTROL FLOW STYLE
580
0000
11 10 9 8 7 6 5 4 3 2 1 0
TM Offs
SDISP/UADDR MO bits 8-0
581
582
0001
TM Offs
CTRlcc MO
21 20 19 18 17
SDISP/UADDR MO bits 3-0
583
584
0010
TM Offs
CTRlcc MO
21 20 19 18 17
?
An MO
15 14 13
585
586
0011
TM Offs
CTRlcc MO
21 20 19 18 17
Vector MO bits 3-0
587
0100
TM Offs
reserved
0101
TM Offs
reserved
0110
TM Offs
reserved
0111
TM Offs
reserved

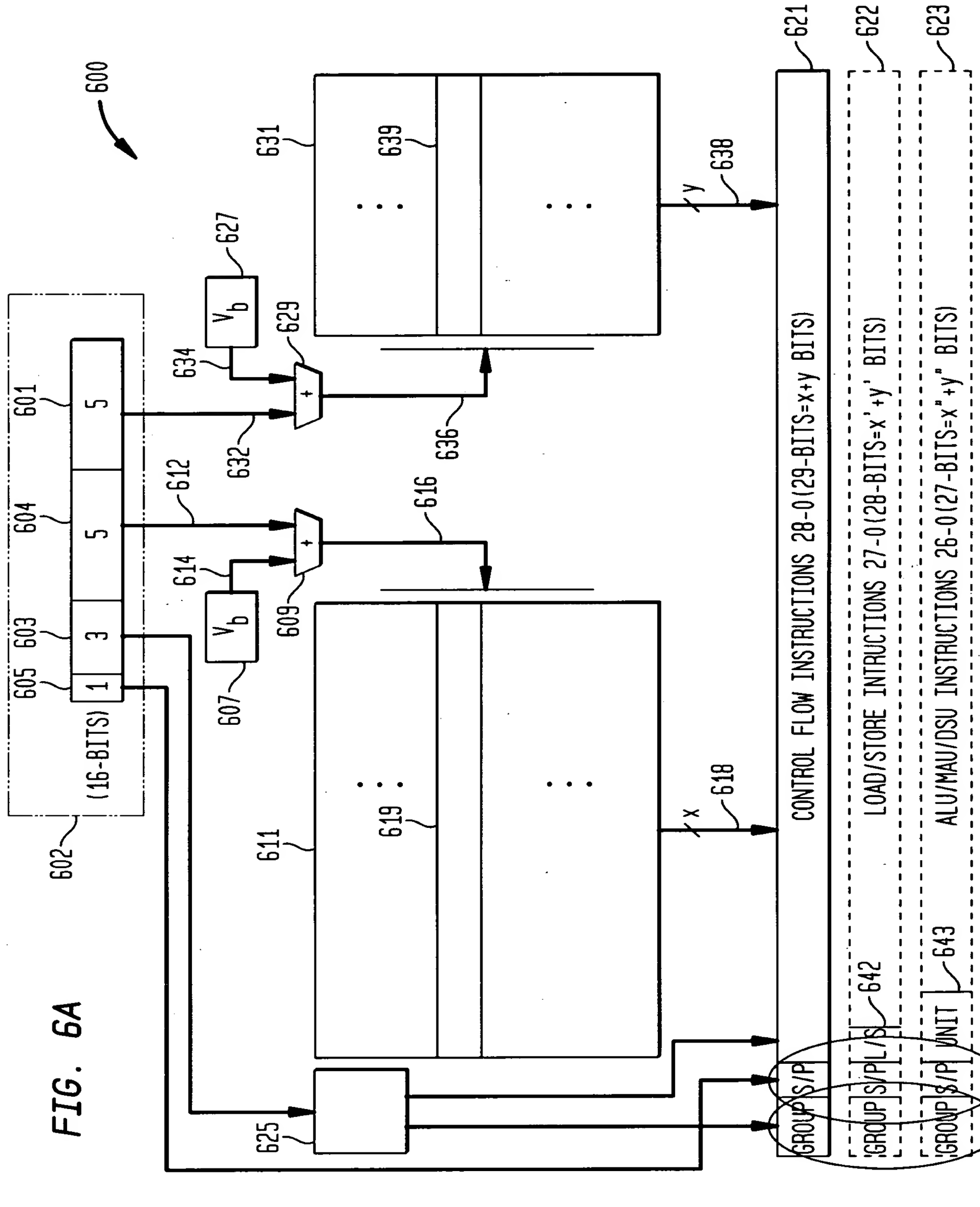

600
631
639
627
621
622
623
638
y
601
604
603
605
(16-BITS)
602
612
614
616
632
634
629
636
609
607
611
619
618
625
CONTROL FLOW INSTRUCTIONS 28-0(29-BITS=x+y BITS)
LOAD/STORE INTRUCTIONS 27-0(28-BITS=x'+y' BITS)
ALU/MAU/DSU INSTRUCTIONS 26-0(27-BITS=x"+y" BITS)
GROUP
S/P
642
643
641
640

FIG. 6A

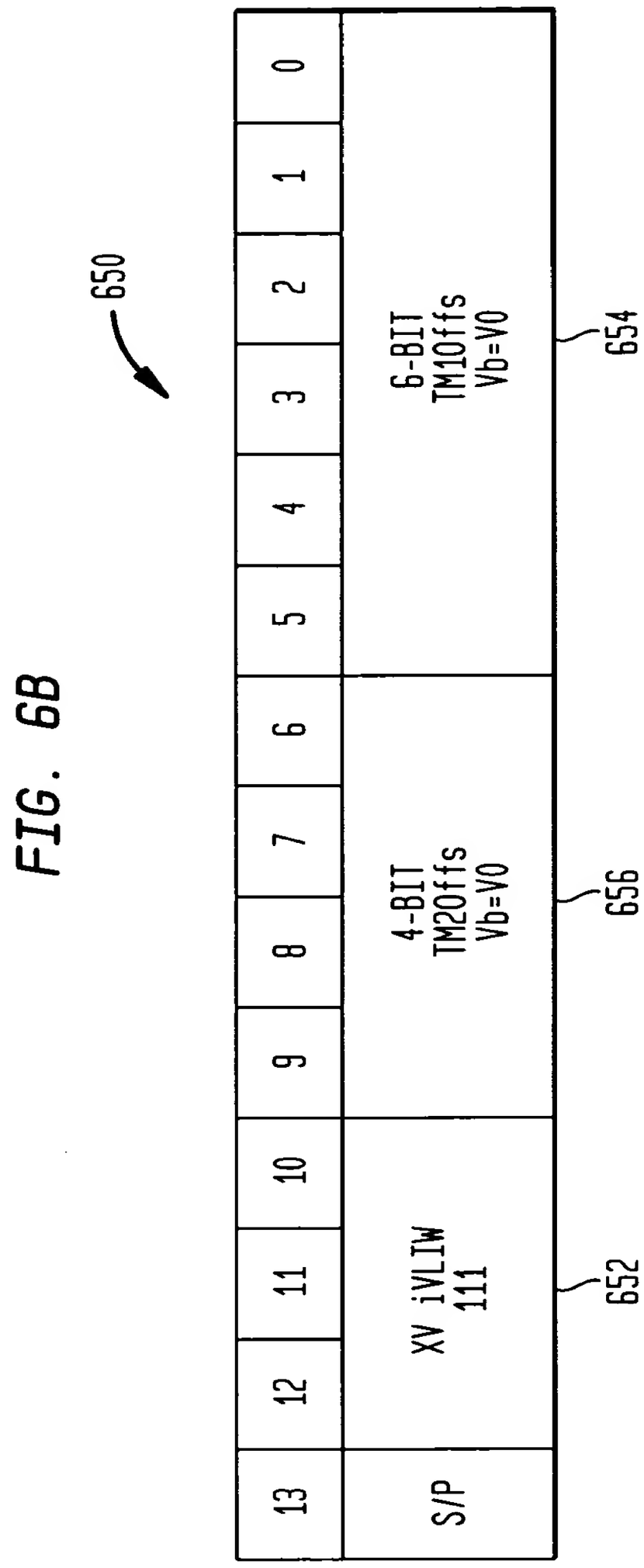

650
0
1
2
3
4
5
6
7
8
9
10
11
12
13
6-BIT
TM10ffs
Vb=V0
654
4-BIT
TM20ffs
Vb=V0
656
XV iVLIW
111
652
S/P

FIG. 6B

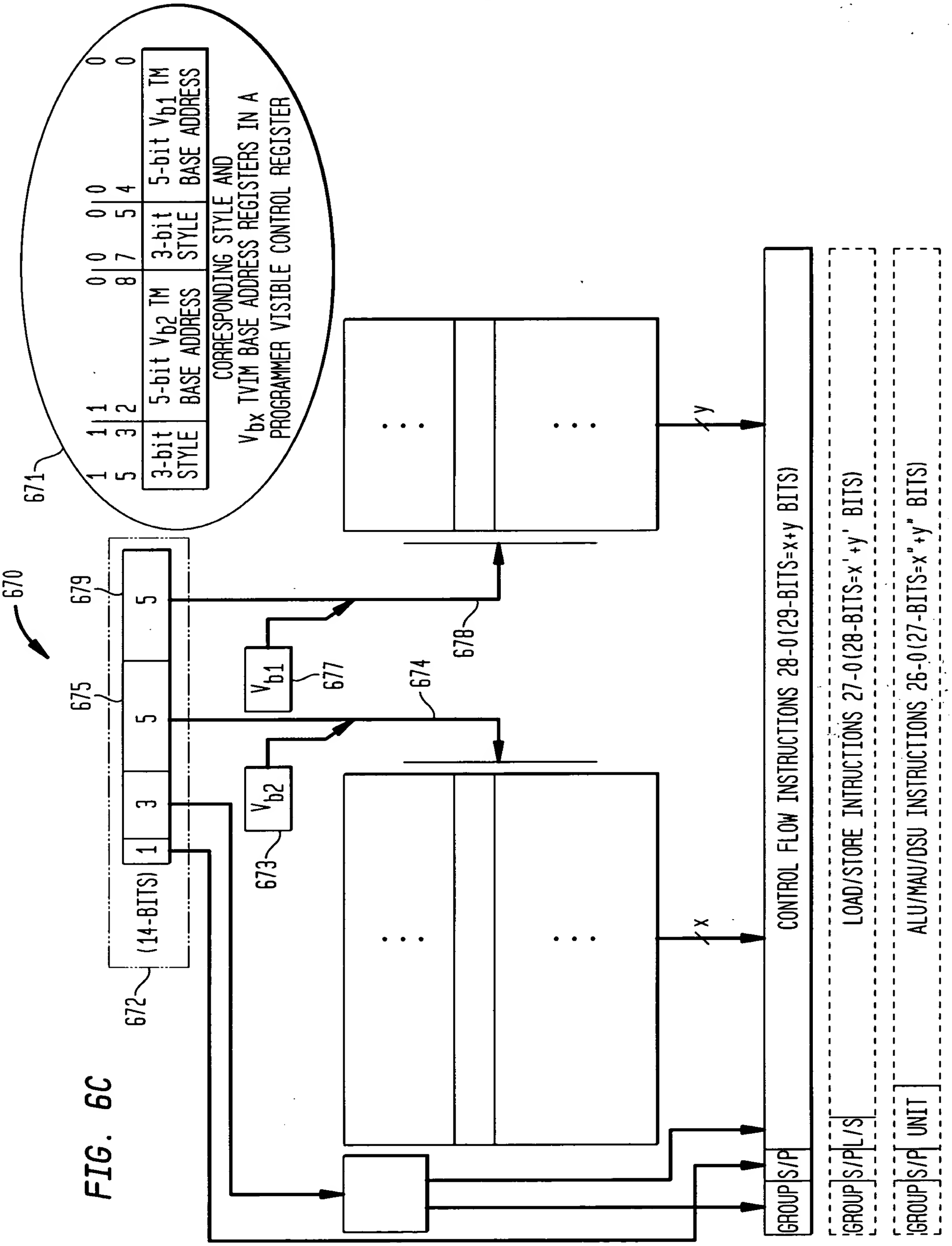

671
1 5 3-bit STYLE
1 3 1 2 5-bit V_{b2} TM BASE ADDRESS
CORRESPONDING STYLE AND
V_{bx} TVIM BASE ADDRESS REGISTERS IN A
PROGRAMMER VISIBLE CONTROL REGISTER
0 0 0 0 0 0
8 7 5 4 3 2 1 0
3-bit STYLE
5-bit V_{b1} TM BASE ADDRESS
670
679
675
673
672
(14-BITS)
1
3
5
5
V_{b1}
V_{b2}
677
674
678
x
y
CONTROL FLOW INSTRUCTIONS 28-0(29-BITS=x+y BITS)
LOAD/STORE INTRUCTIONS 27-0(28-BITS=x'+y' BITS)
ALU/MAU/DSU INSTRUCTIONS 26-0(27-BITS=x"+y" BITS)
GROUP S/P
GROUP S/P L/S
GROUP S/P UNIT

FIG. 6C

FIG. 7

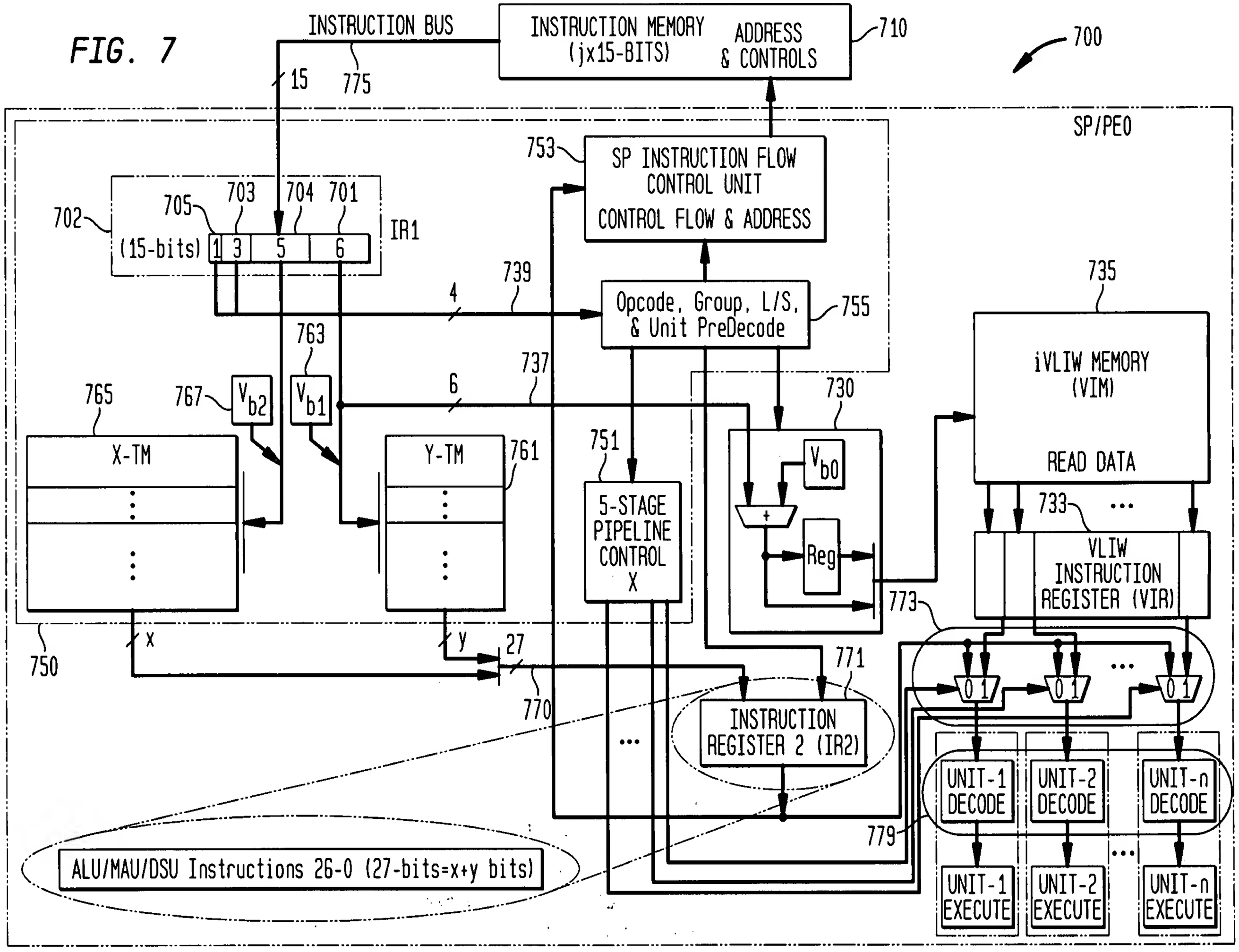
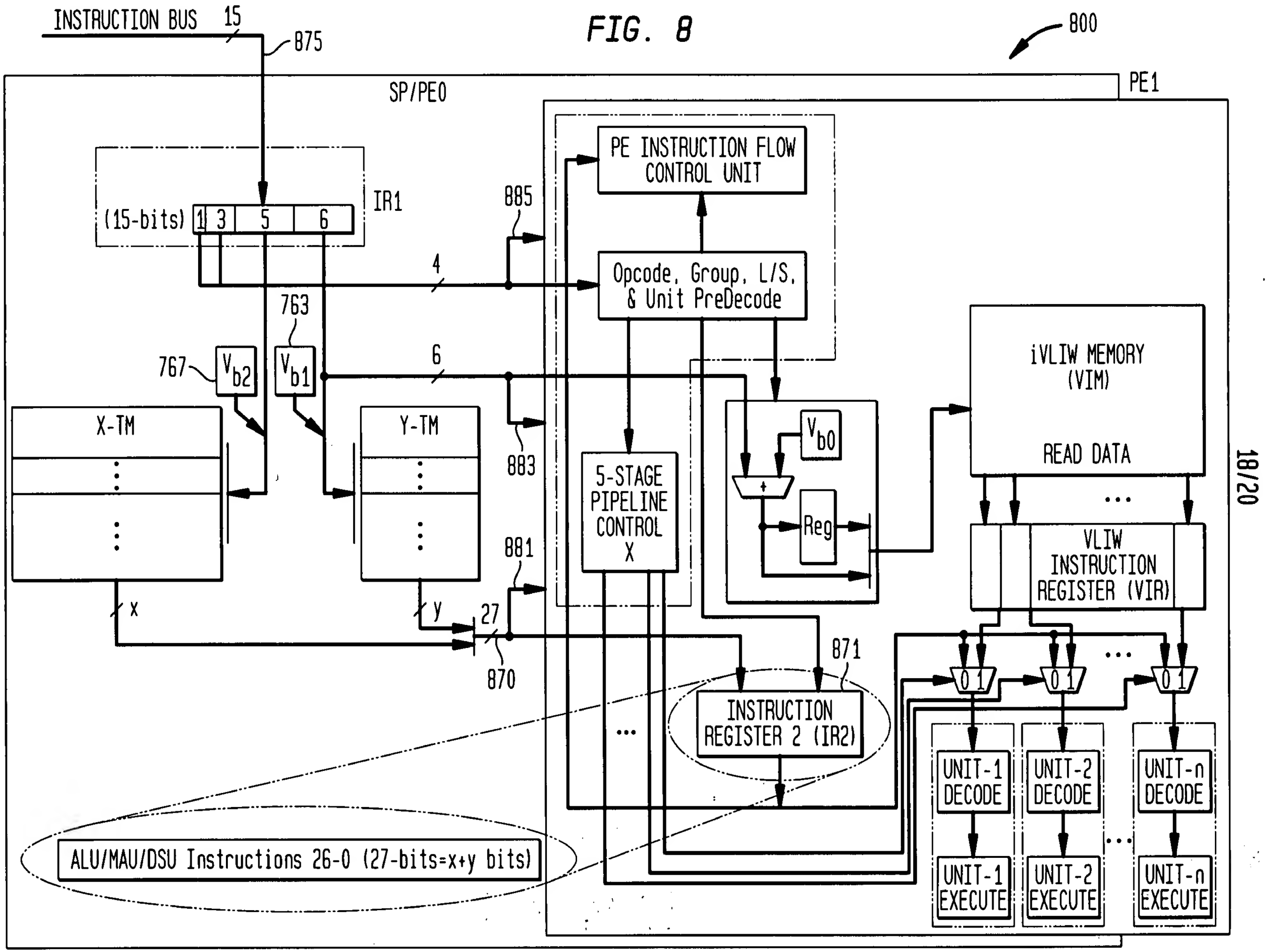

INSTRUCTION BUS
INSTRUCTION MEMORY (jx15-BITS)
ADDRESS & CONTROLS
710
700
15
775
SP/PE0
753
SP INSTRUCTION FLOW CONTROL UNIT
CONTROL FLOW & ADDRESS
705
703
704
701
702
(15-bits)
1
3
5
6
IR1
739
4
Opcode, Group, L/S, & Unit PreDecode
755
735
763
737
6
730
765
767
V_{b2}
V_{b1}
iVLIW MEMORY (VIM)
READ DATA
751
X-TM
Y-TM
761
V_{b0}
+
Reg
5-STAGE PIPELINE CONTROL X
733
VLIW INSTRUCTION REGISTER (VIR)
773
750
x
y
27
771
770
INSTRUCTION REGISTER 2 (IR2)
0 1
UNIT-1 DECODE
UNIT-2 DECODE
UNIT-n DECODE
779
UNIT-1 EXECUTE
UNIT-2 EXECUTE
UNIT-n EXECUTE
ALU/MAU/DSU Instructions 26-0 (27-bits=x+y bits)

FIG. 8


INSTRUCTION BUS
15
875
800
SP/PE0
PE1
PE INSTRUCTION FLOW CONTROL UNIT
IR1
(15-bits)
1
3
5
6
885
4
Opcode, Group, L/S, & Unit PreDecode
763
767
V_{b2}
V_{b1}
6
X-TM
Y-TM
883
5-STAGE PIPELINE CONTROL X
V_{b0}
Reg
iVLIW MEMORY (VIM)
READ DATA
VLIW INSTRUCTION REGISTER (VIR)
881
x
y
27
870
871
INSTRUCTION REGISTER 2 (IR2)
0 1
UNIT-1 DECODE
UNIT-2 DECODE
UNIT-n DECODE
UNIT-1 EXECUTE
UNIT-2 EXECUTE
UNIT-n EXECUTE
ALU/MAU/DSU Instructions 26-0 (27-bits=x+y bits)

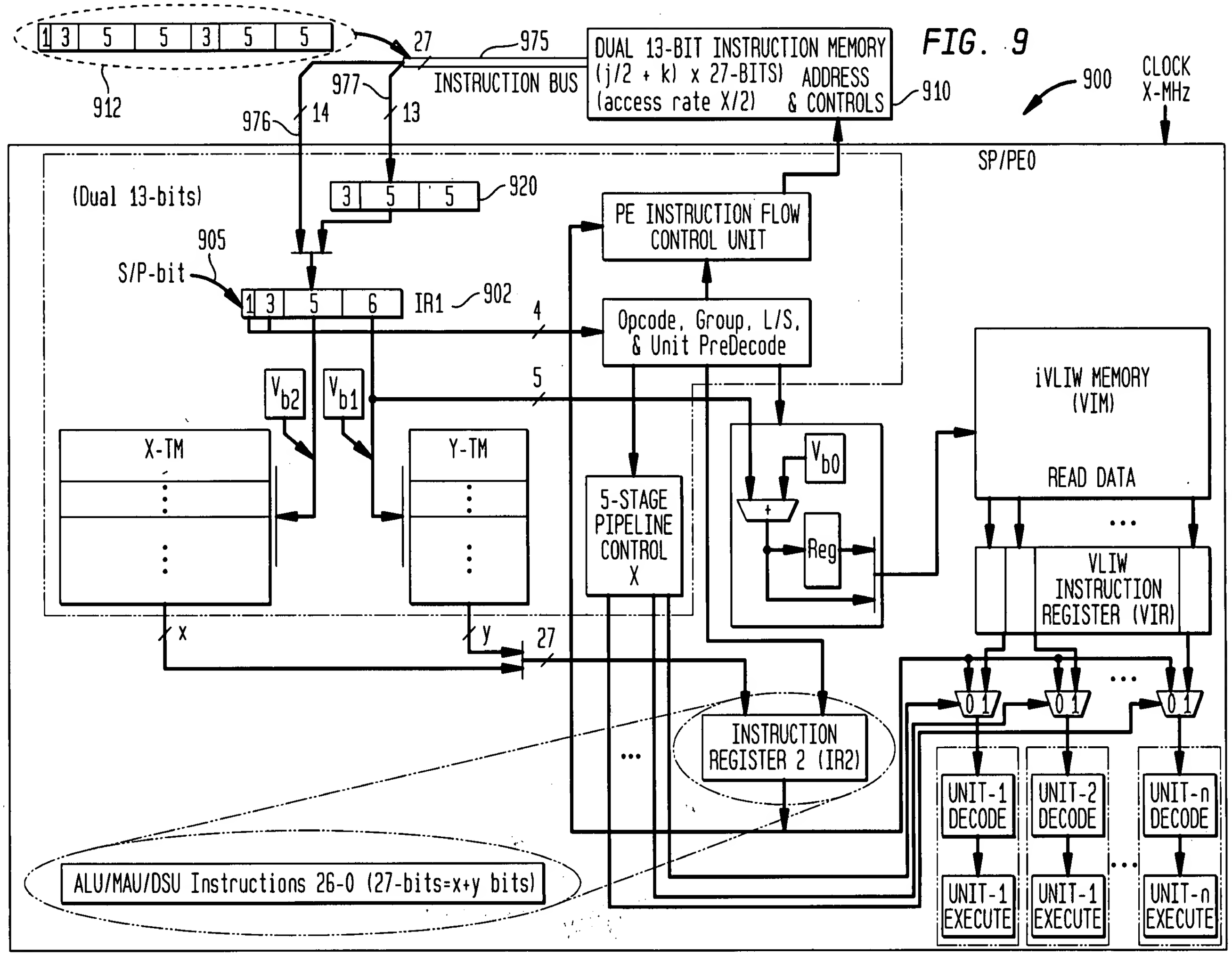

1 3 5 5 3 5 5
912
27
975
INSTRUCTION BUS
977
976
14
13
DUAL 13-BIT INSTRUCTION MEMORY
(j/2 + k) x 27-BITS)
(access rate X/2)
ADDRESS
& CONTROLS
910
900
CLOCK
X-MHz
SP/PE0
(Dual 13-bits)
3 5 5
920
905
S/P-bit
1 3 5 6
IR1
902
4
PE INSTRUCTION FLOW
CONTROL UNIT
Opcode, Group, L/S,
& Unit PreDecode
5
V_{b2}
V_{b1}
V_{b0}
X-TM
Y-TM
5-STAGE
PIPELINE
CONTROL
X
+
Reg
iVLIW MEMORY
(VIM)
READ DATA
VLIW
INSTRUCTION
REGISTER (VIR)
x
y
27
0 1
INSTRUCTION
REGISTER 2 (IR2)
UNIT-1
DECODE
UNIT-2
DECODE
UNIT-n
DECODE
UNIT-1
EXECUTE
UNIT-1
EXECUTE
UNIT-n
EXECUTE
ALU/MAU/DSU Instructions 26-0 (27-bits=x+y bits)

FIG. 9

FIG. 10

1000

	1015 CYCLE	1025 FETCH	1035 Xpand & Dispatch	1045 Decode	1055 Execute	1065 Cond. Ret
1010	i	SP Fetches a B-bit Instr(i)=ADD.S instruction & loads it into IR1	Previous Instruction Instr(i-1)	Previous Instruction Instr(i-2)	Previous Instruction Instr(i-3)	Previous Instruction Instr(i-4)
1020	i+1	SP Fetches a B-bit Instr(i+1)=XV.S instruction & loads it into IR1	S/P-bit indicates an SP only operation. Local TM fetches occur and a native form of the Instr(i)=ADD.S instruction is loaded into IR2. The S/P-bit and 3-bit opcode are decoded in the S/P.	Previous Instruction Instr(i-1)	Previous Instruction Instr(i-2)	Previous Instruction Instr(i-3)
1030	i+2	SP Fetches a B-bit Instr(i+2)=COPY.S instruction & loads it into IR1	S/P-bit opcode indicate an SP XV operation. Local TM fetches occur and a native form of the Instr(i+1)=XV.S instruction is loaded into IR2. The S/P-bit, and 3-bit opcode are decoded in the S/P. The VIM address is calculated and the iVLIW is fetched from the XV VIM	The ALU decodes Instr(i)=ADD.S instruction	Previous Instruction Instr(i-1)	Previous Instruction Instr(i-2)
1040	i+3	SP Fetches a B-bit Instr(i+3)=ADD.S instruction & loads it into IR1	S/P-bit indicates an SP only operation. Local TM fetches occur and a native form of the Instr(i+2)=COPY.S instruction is loaded into IR2	Instr(i+1)=XV.S causes up to 5 instructions in iVLIW decode	The ALU executes Instr(i)=ADD.S instruction	Previous Instruction Instr(i-1)
1050	i+4	SP Fetches a B-bit instruction: Instr(i+4)	S/P-bit indicates an SP only operation. Local TM fetches occur and a native form of the Instr(i+3)=ADD.S instruction is loaded into IR2	The DSU decodes the Instr(i+2)=COPY.S instruction	Instr(i+1)=XV.S causes up to 5 instructions in iVLIW execute	Instr(i+1)=ADD.S side effects are set in ASFs and ACFs